

# PATENT ABSTRACTS OF JAPAN

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**(21)Application number : 11-035391**

**(71)Applicant : HITACHI LTD**

**(22)Date of filing : 15.02.1999**

(72)Inventor : KURODA KENICHI

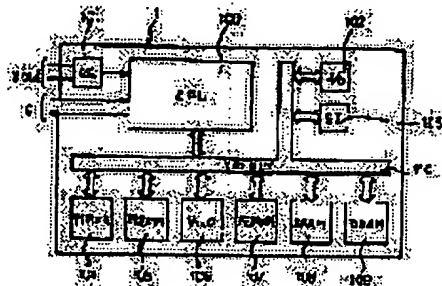
## (54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

**(57) Abstract**

**PROBLEM TO BE SOLVED:** To improve the functions of a semiconductor integrated circuit device which is made of a single-chip microcomputer.

**SOLUTION:** A CPU 100, a SRAM 108 and a DRAM 109 are integrated on the same semiconductor substrate.

Next, the SRAM 108 is used for rapid data transfer in a small capacity, while the DRAM 109 is used for slow data transfer but in a large memory capacity, so that a RAM which obviates the mutual defects of the SRAM 108 hard to have the large capacity as well as the slow transfer velocity of the DRAM 109 can be obtained.



## LEGAL STATUS

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**[Date of sending the examiner's decision of rejection] 13.06.2000**

**[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]**

**[Date of final disposal for application]**

[Patent number] 3358719

**[Date of registration]** 11.10.2002

**[Number of appeal against examiner's decision of rejection] 2000-10566**

**[Date of requesting appeal against examiner's 12.07.2000**

**\* NOTICES \***

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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**CLAIMS**

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[Claim(s)]

[Claim 1] Semiconductor integrated circuit equipment characterized by accumulating CPU, and SRAM and DRAM on the same semiconductor substrate.

[Claim 2] Semiconductor integrated circuit equipment according to claim 1 characterized by Above CPU containing a control section, operation part, and a register at least.

[Claim 3] Semiconductor integrated circuit equipment according to claim 1 or 2 characterized by connecting Above SRAM with Above CPU through an internal bus, and operating as a cache memory.

[Claim 4] Semiconductor integrated circuit equipment given in any 1 term of the claim 1 characterized by the capacity of Above SRAM being smaller than the capacity of Above DRAM, or a claim 3.

[Claim 5] Above CPU, Above SRAM, and Above DRAM are semiconductor integrated circuit equipment given in any 1 term of the claim 1 characterized by connecting mutually through an internal bus, or a claim 4.

[Claim 6] Semiconductor integrated circuit equipment which DRAM is formed in the 1st field of the same base, SRAM is formed in the 2nd field, and CMISFET is formed in the 3rd field, and is characterized by the capacity of Above DRAM being larger than the capacity of SRAM.

[Claim 7] Above CMISFET is semiconductor integrated circuit equipment according to claim 6 characterized by constituting some circuits of CPU at least.

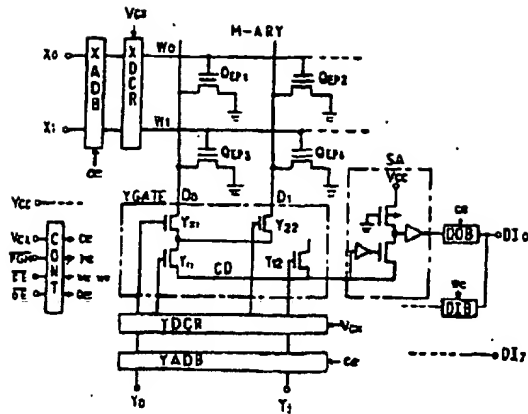
[Claim 8] Semiconductor integrated circuit equipment according to claim 6 or 7 characterized by forming the gate electrode of NMISFET of Above SRAM, and the gate electrode of Above CMISFET of the same conductor layer.

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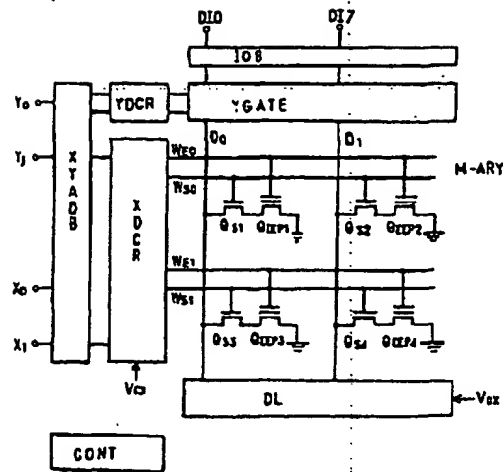
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図 3



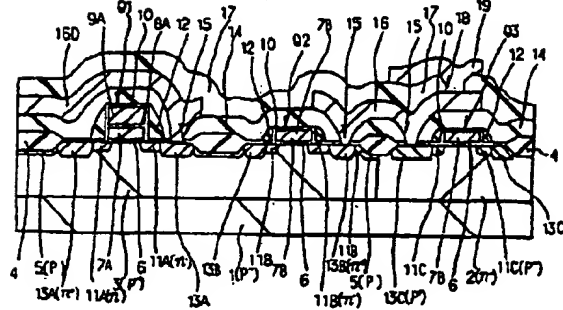
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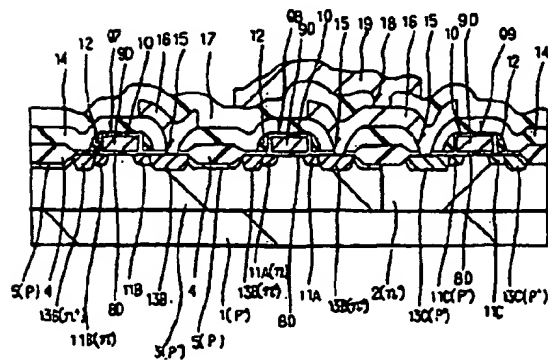
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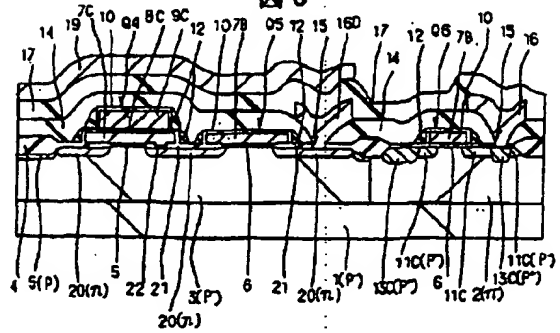
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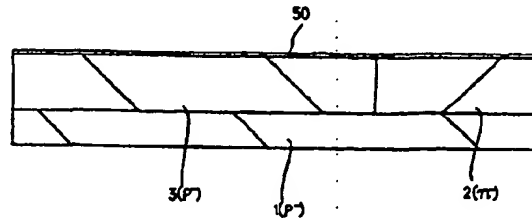
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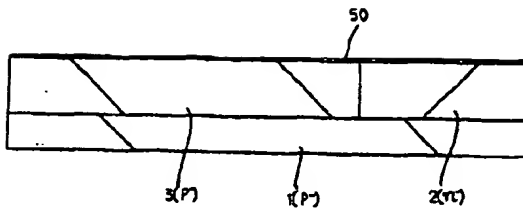
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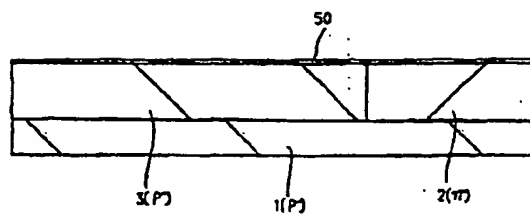
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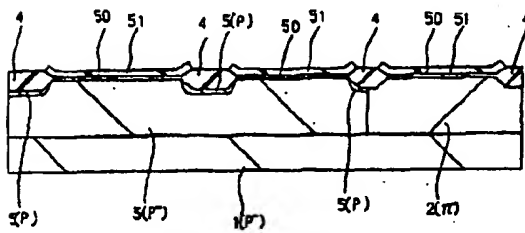
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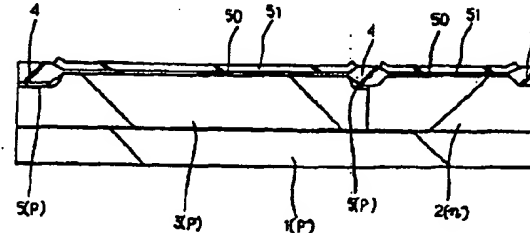
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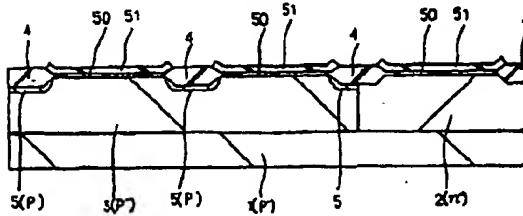
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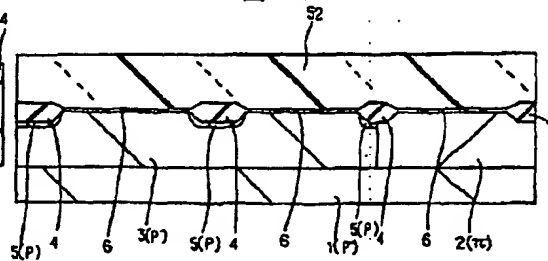
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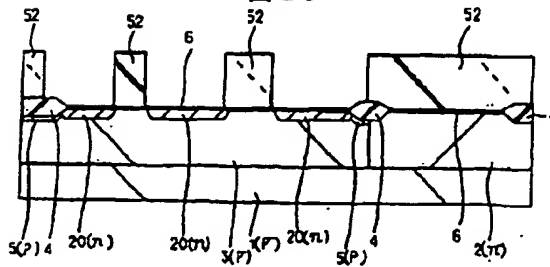
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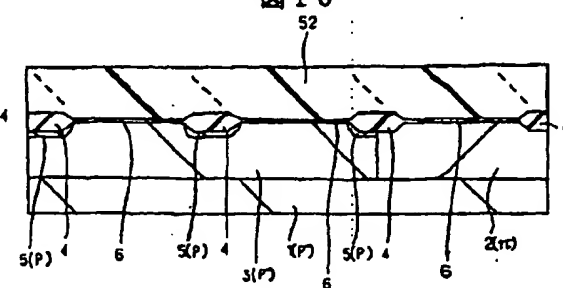
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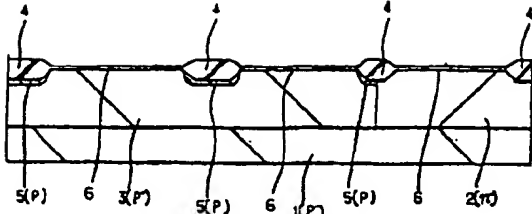
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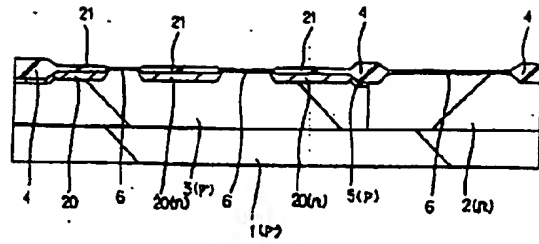
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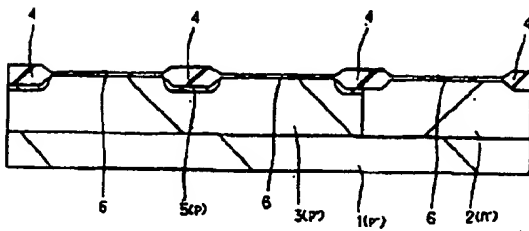
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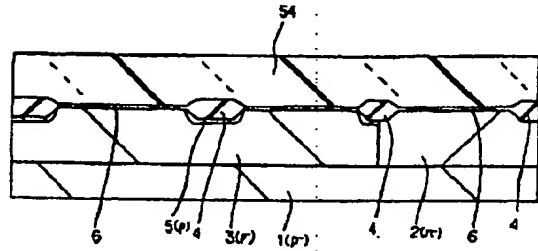
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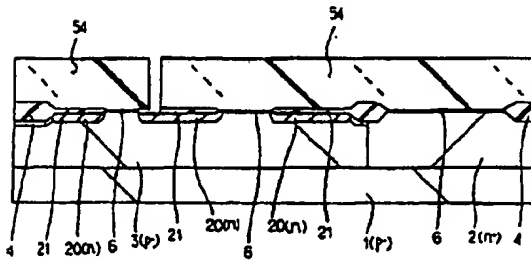
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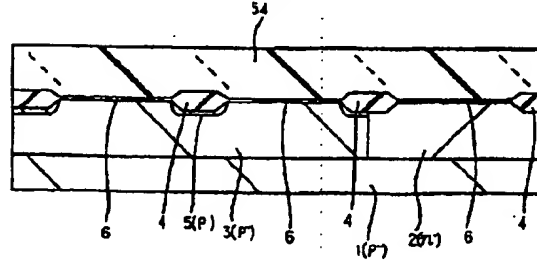
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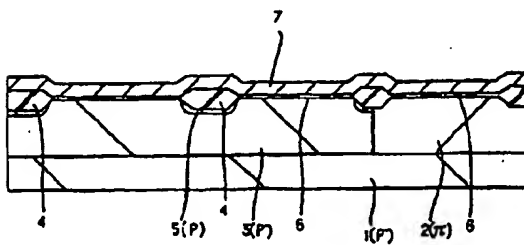
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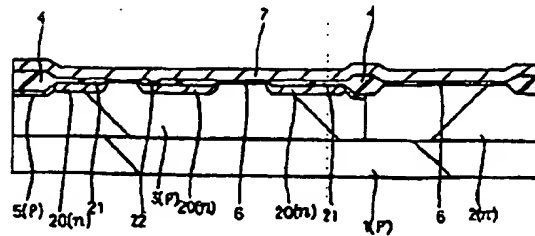
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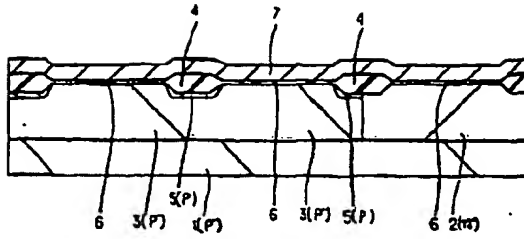
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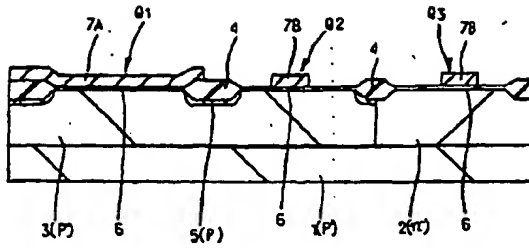
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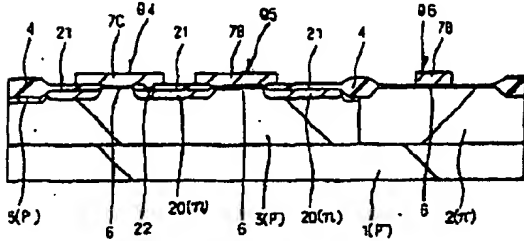
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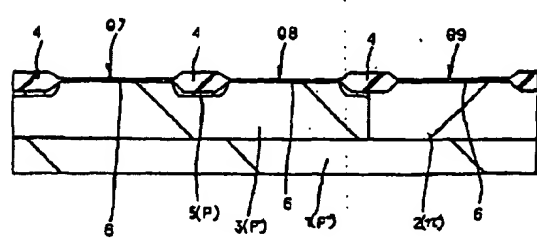
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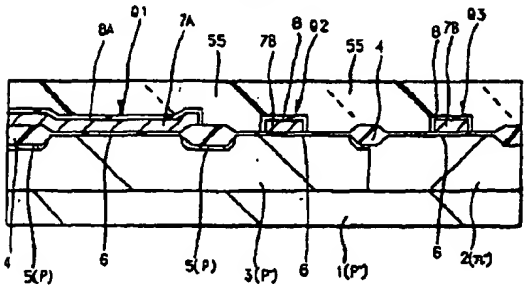
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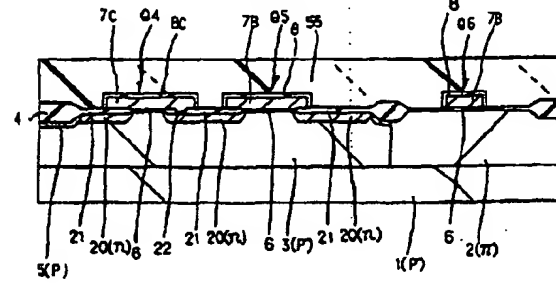
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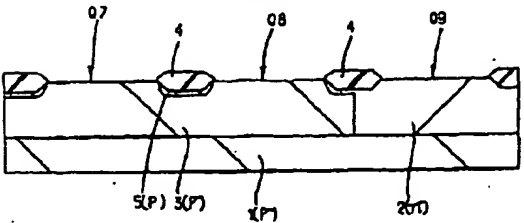
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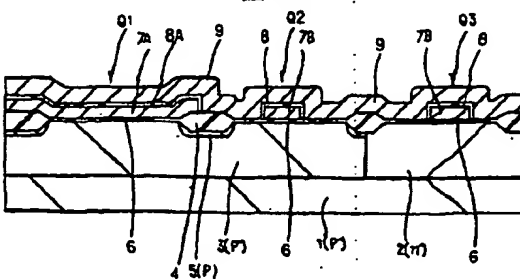
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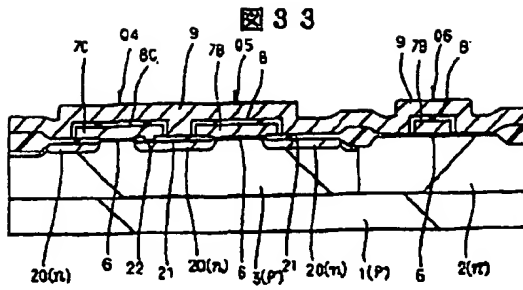


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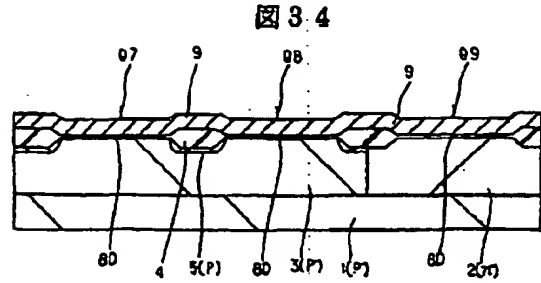
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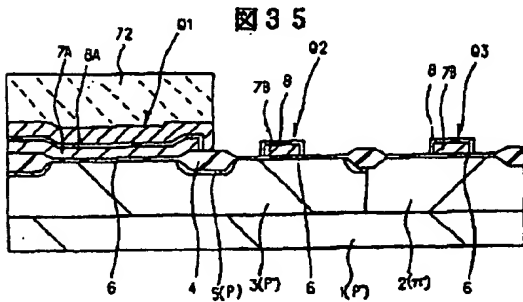
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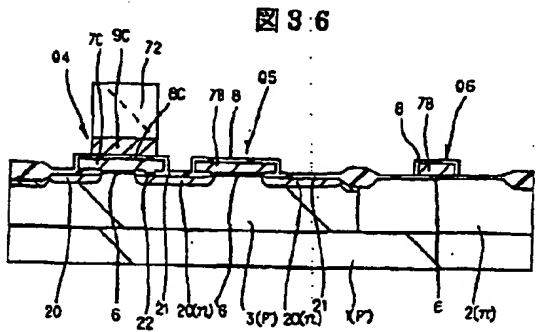
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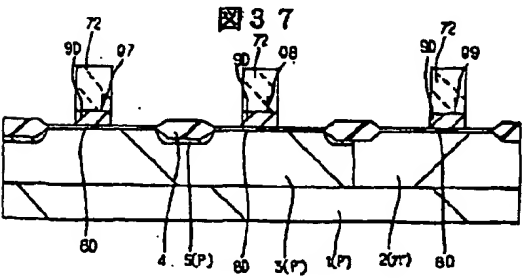
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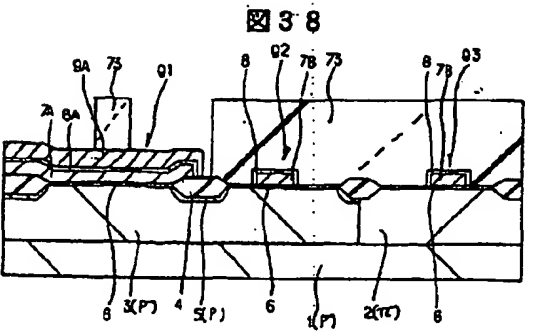
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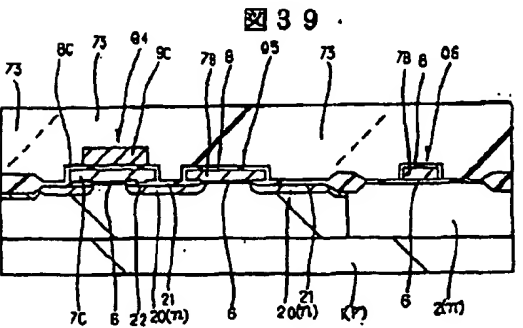
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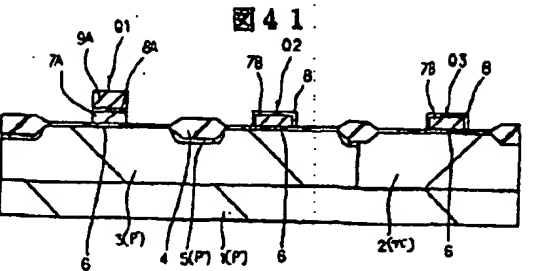
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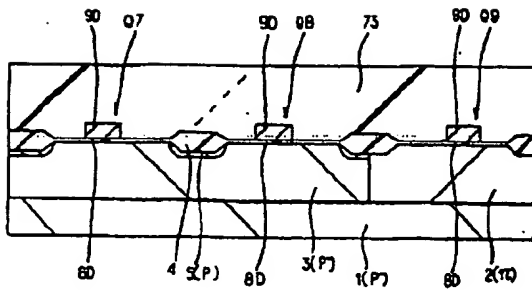


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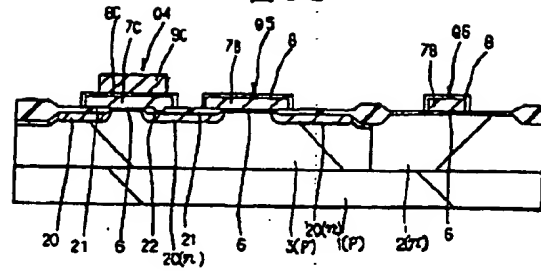
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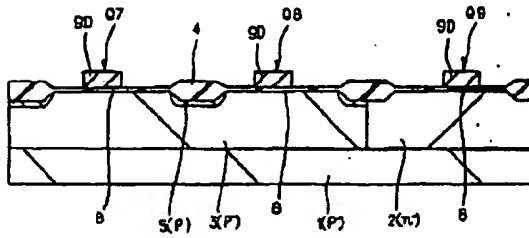
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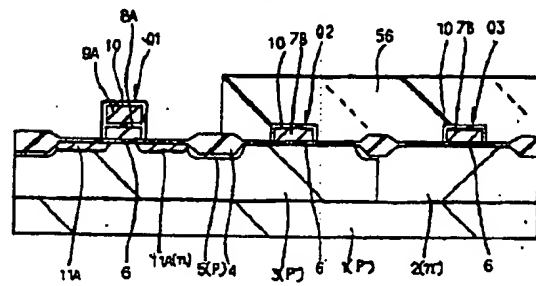
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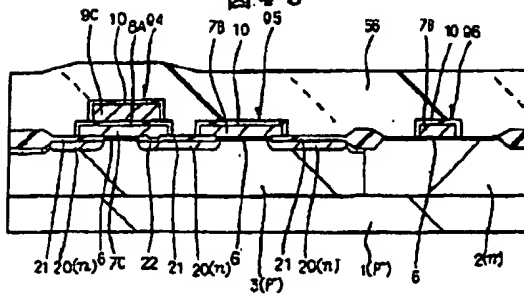
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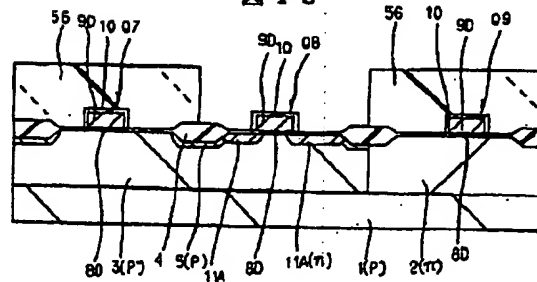
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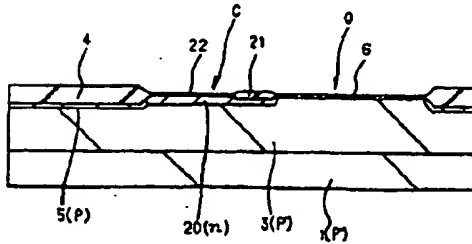
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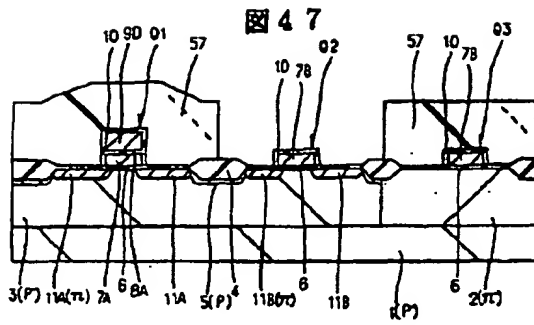


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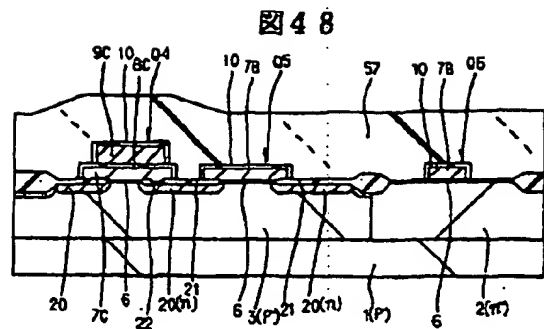
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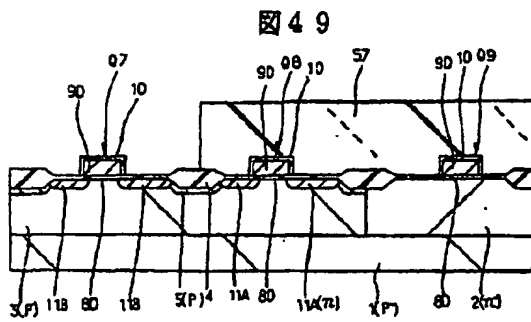
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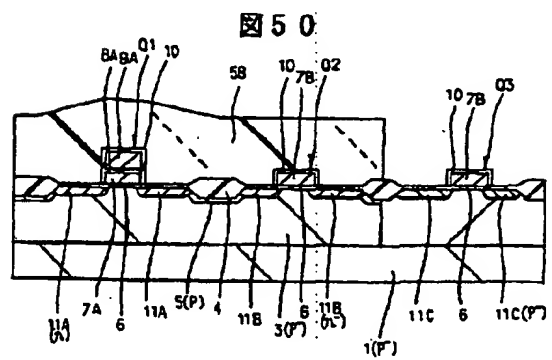
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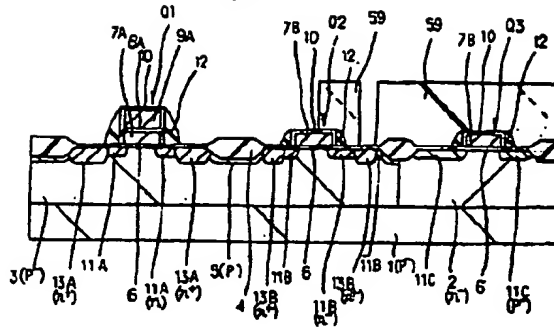


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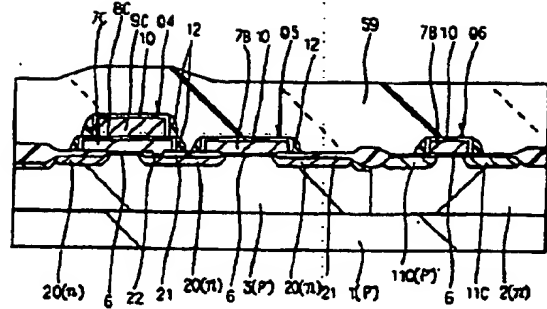
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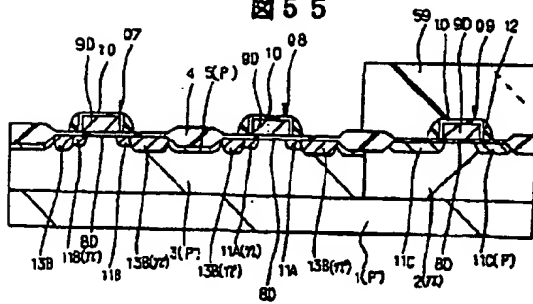
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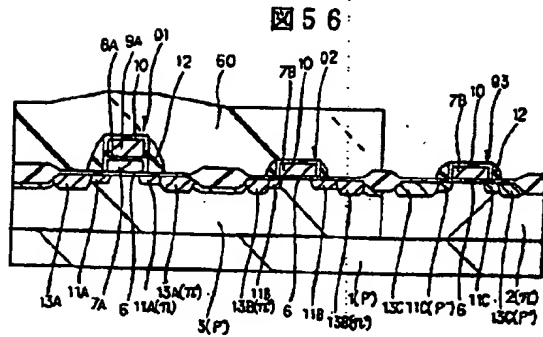
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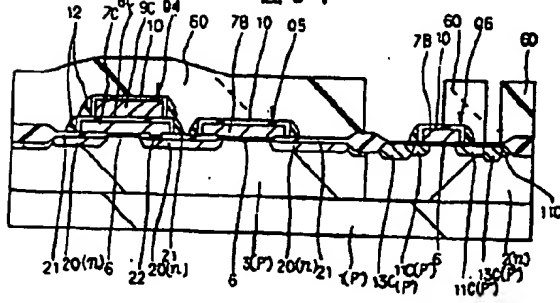
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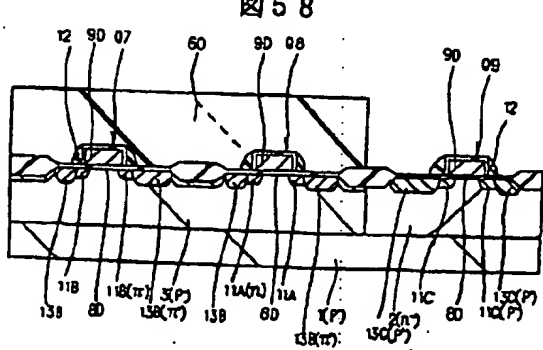
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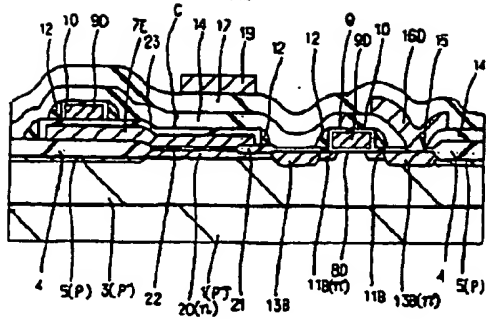
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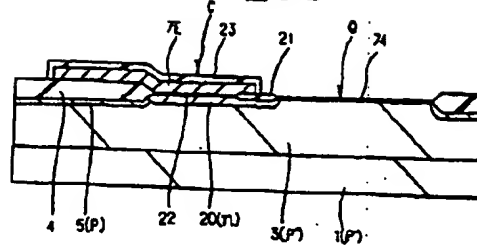
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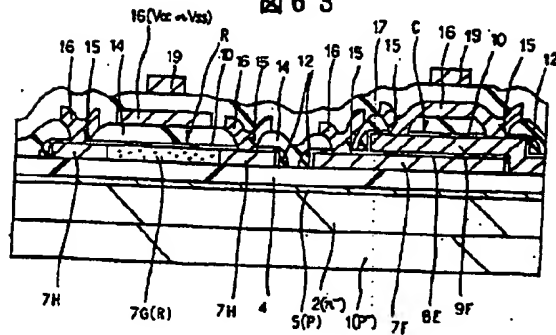
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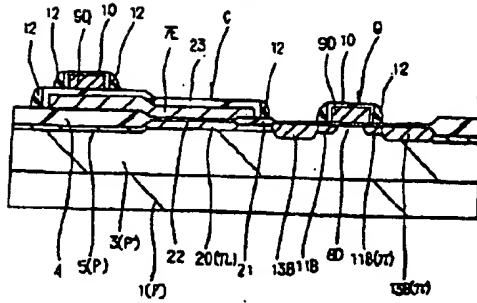
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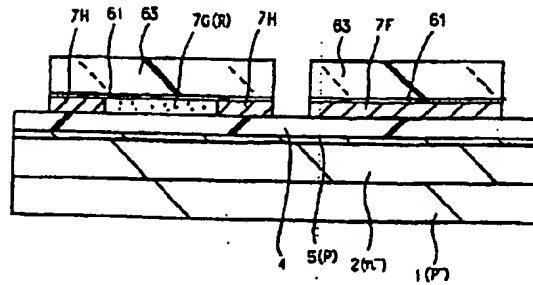
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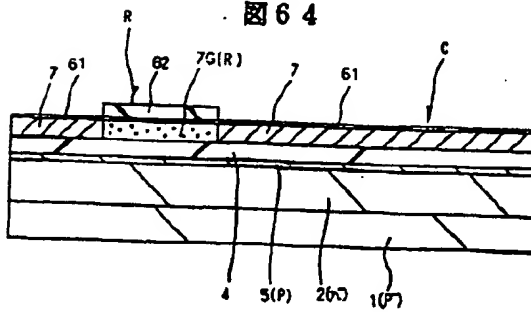
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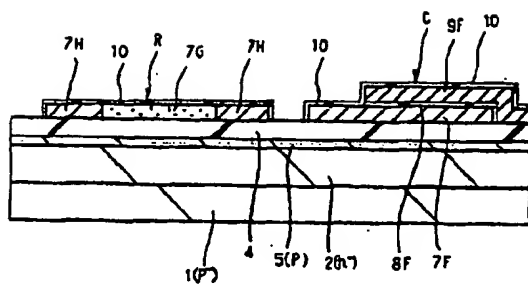
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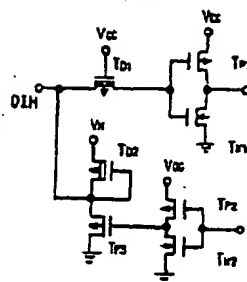
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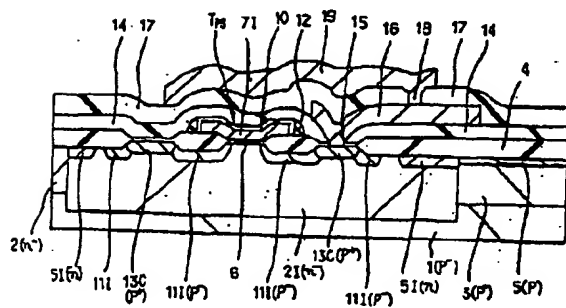
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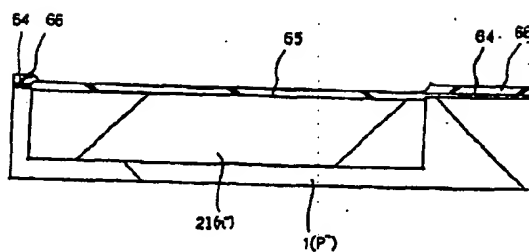
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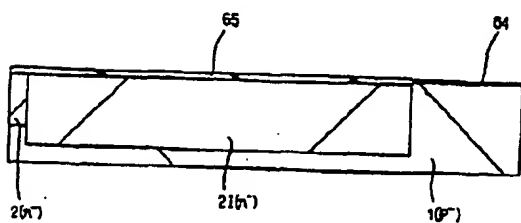
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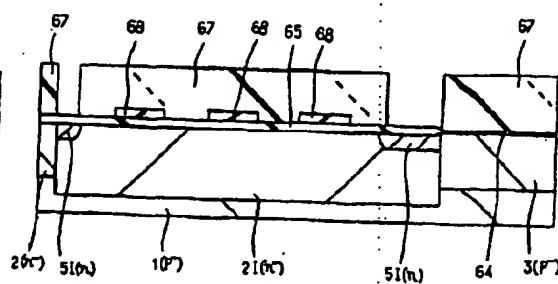
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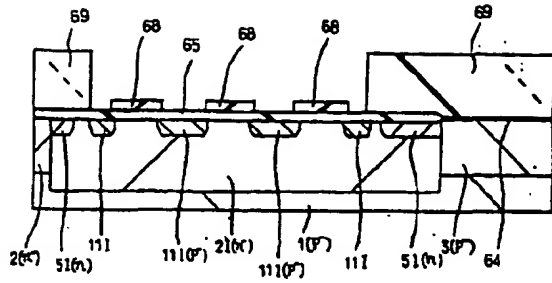
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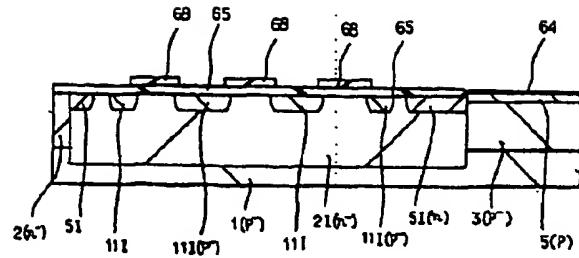
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図 7 2



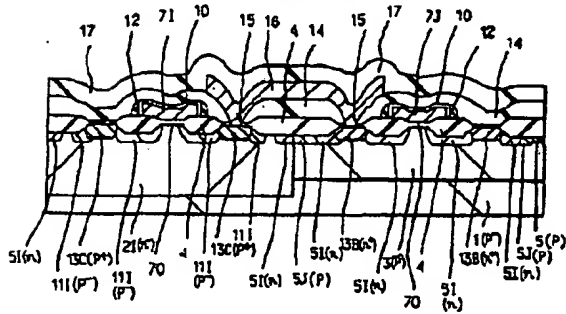
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図 7 3



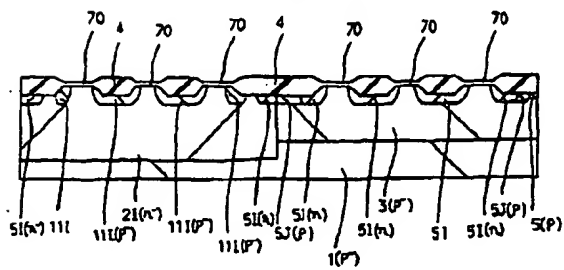
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図 7 4

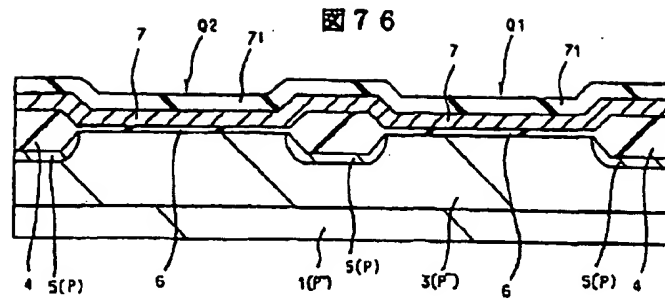


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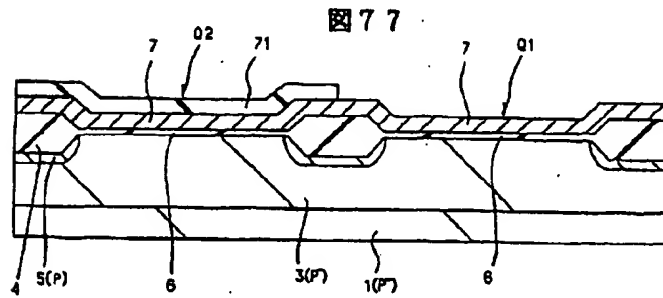
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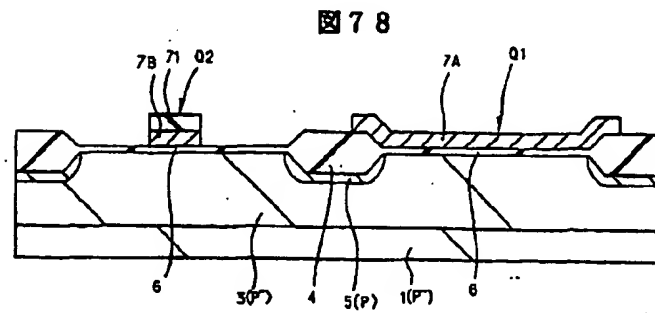
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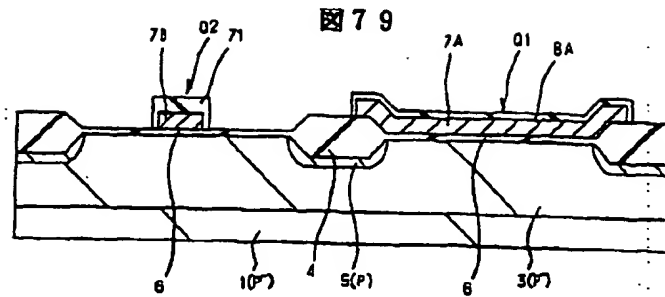
【図 77】



【図 78】

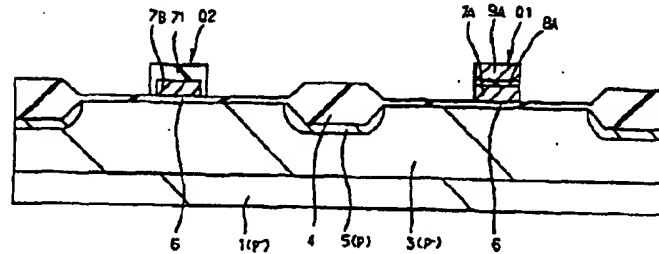


【図 79】



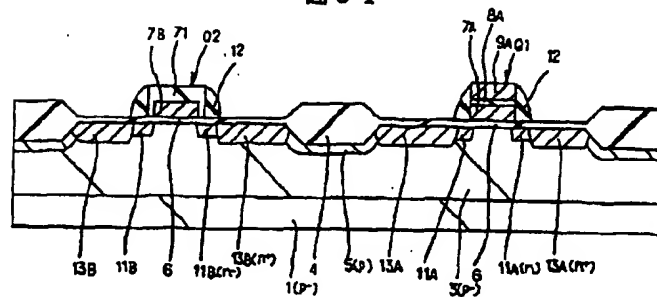
【図 80】

図 80



【図 81】

図 81



## 【手続補正書】

【提出日】平成 11 年 6 月 22 日

【手続補正 1】

【補正対象書類名】明細書

【補正対象項目名】図面の簡単な説明

【補正方法】変更

【補正内容】

【図面の簡単な説明】

【図 1】本発明の一実施の形態である半導体集積回路装置のマイクロコンピュータを示すブロック図である。

【図 2】図 1 に示したマイクロコンピュータが備えている SRAM 108 のメモリセルの等価回路図である。

【図 3】前記マイクロコンピュータに搭載されている EPROM 105 の概略構成を示す等価回路図である。

【図 4】前記マイクロコンピュータに搭載されている EEPROM 107 の概略構成を示す等価回路図である。

【図 5】前記マイクロコンピュータの EPROM、EEPROM 及び CPU 等の論理部を構成する MISFET の製造工程における断面図である。